REMARKS

This communication is in response to the Office Action dated January 26, 2006. Claims 1-10, 13-20, 22 and 23 are pending in the present Application. Claims 11, 12, 21 and 24-30 have been withdrawn from consideration. Claims 1-10, 13-20, 22 and 23 are rejected.

§102 Rejections

Claims 1-10, 13-20, 22 and 23

For ease of review, Applicant reproduces independent claims 1 and 13 herein below:

1. A method for forming a semiconductor device comprising:

forming a 3-dimensional (3D) pattern in a substrate; and

depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device.

13. A system for forming a semiconductor device comprising:

means for forming a 3-dimensional (3D) pattern in a substrate; and

means for depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device.

The Examiner states:

> **Claims 1-2, 5-6, 9-10, 13, 15-16 and 18-20 are rejected under 35 USC §102(e) as being anticipated by Hasegawa et al. (US 2004/0023162).**

Applicant respectfully disagrees. The present invention includes a method and system for forming a semiconductor device. Varying embodiments allow 2-

dimensional alignment features to be created in 3-dimensional structures on a device substrate prior to any processing steps. Subsequent processing steps, including material deposition, planarization and anisotropic etching are utilized to construct a multi-level aligned pattern. Accordingly, the use of the method and system can potentially increase the flexibility of the semiconductor manufacturing process.

Claim 1 recites a method for forming a semiconductor device that includes forming a 3-dimensional (3D) pattern in a substrate and depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device.

The Examiner states that the Hesegawa reference anticipates the present invention. Applicant respectfully disagrees and asserts that the Hesegawa reference does not disclose depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device as recited in claim 1 of the present invention. Hesegawa discloses a stamper that includes a substrate and a plurality of protrusions of different heights formed on one of the surfaces of the substrate, the protrusions of larger height having a stack structure formed of at least two layers of at lease two types of materials, thereby transferring a plurality of patterns at the same time.

The Examiner stipulates that Hesegawa teaches these steps in Figures 10A-10L of Hesegawa (see attached Exhibit A). These Figures are described in Hesegawa in paragraph 49. Paragraph 49 of Hesegawa reads:

> FIGS. 10A to 10L are diagrams for explaining the steps of fabricating a multilayer wiring substrate. First, as shown in FIG. 10A, a resist 702 is formed on the surface of a multilayer wiring substrate 1001 configured of a silicon oxide film 1002 and a copper wire 1003, after which a pattern is transferred by a stamper (not shown). The exposed areas 703 of the multilayer wiring substrate 1001 are dry-etched with CF.sub.4/H.sub.2 gas. As shown in FIG. 10B, each

> exposed area 703 is processed into the shape of a channel in the surface of the multilayer wiring substrate 1001. The resist 702 is etched by RIE to remove the low-stepped portions of the resist 702. As shown in FIG. 10C, the exposed areas 703 are enlarged. Under this condition, the exposed areas 703 are dry-etchd until the channels already formed reach the depth of the copper wire 1003. Thus, the structure shown in FIG. 10D is obtained. By removing the resist 702, the multilayer substrate 1001 having channel-shaped grooves in the surface thereof is obtained as shown in FIG. 10E. After forming a metal film by sputtering on the surface of the multilayer wiring substrate 1001 (not shown), a metal plated film 1004 is formed by electrolytic plating, as shown in FIG. 10F. After that, the metal plated film 1004 is polished until the silicon oxide film 1002 of the multilayer wiring substrate 1001 is exposed. As shown in FIG. 10G, the multilayer wiring substrate 1001 having a metal wiring in the surface thereof is obtained.

Applicant fails to see how this paragraph demonstrates the steps of forming a 3-dimensional (3D) pattern in a substrate and depositing at least one material over the substrate in accordance with desired characteristics of the semiconductor device as recited in claim 1 of the present invention. The Examiner states that Hesegawa discloses the step of forming a 3D pattern (resist 702) in a substrate (1001) and depositing at least one material (material layer 1002) over the substrate (1001) in accordance with the desired characteristics of the semiconductor device. (See attached Exhibit A).

Applicant respectfully disagrees and asserts that the Examiner aforementioned assertion is incorrect. Hesegawa does not disclose depositing at least one material over the substrate in accordance with the desired characteristics of the semiconductor device as recited in claim 1 of the present invention. As can be seen in exhibit A, the substrate 1001 is made up of an oxide film 1002 and a copper wire 1003. Accordingly, the oxide film 1002 is not deposited over the substrate 1001. The oxide film 1002 is what the substrate 1001 is comprised of. Consequently, Hesegawa does not disclose depositing at least one material over

the substrate in accordance with the desired characteristics of the semiconductor device as recited in claim 1 of the present invention.

Since the Hesegawa reference does not disclose depositing at least one material over the substrate in accordance with the desired characteristics of the semiconductor device as recited in claim 1 of the present invention, claim 1 of the present invention is allowable over the Hesegwa reference. Furthermore, claim 12 discloses similar features of claim 1 and should also be deemed allowable over the Hesegwa reference.

Claims 2, 5-6, 9-10, 15-16 and 18-20

Since claims 2, 5-6, 9-10, 15-16 and 18-20 are respectively dependent on claims 1 and 13, the above-articulated arguments with regard to independent claims 1 and 13 apply with equal force to claims 2, 5-6, 9-10, 15-16 and 18-20. Accordingly, claims 2, 5-6, 9-10, 15-16 and 18-20 should be allowed over the Examiner's cited reference.

§103 Rejections

Claims 3-4, 7-8, 14, 17 and 22-23

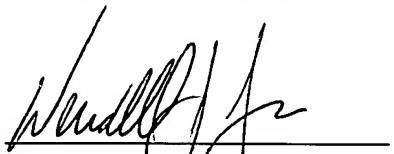
Since claims 3-4, 7-8, 14, 17 and 22-23 are respectively dependent on claims 1 and 13, the above-articulated arguments with regard to independent claims 1 and 13 apply with equal force to claims 3-4, 7-8, 14, 17 and 22-23.

Accordingly, claims 3-4, 7-8, 14, 17 and 22-23 should be allowed over the Examiner's cited references.

Alternatively, if the Examiner is not persuaded by the above delineated arguments, Applicant has included a Rule 1.131 affidavit for the purpose of swearing behind the Hesegawa reference. The affidavit is such, in character and weight, as to establish the conception of the invention prior to the effective date of the Hesegawa reference coupled with due diligence from prior to that date to the filing of the application. As a result of this showing, Applicant asserts that the Hesegawa reference is antedated and should not bar the granting of a patent to the Applicant.

Applicant believes that this application is in condition for allowance. Accordingly, Applicant respectfully requests reconsideration, allowance and passage to issue of the claims as now presented. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,



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